

REMARKS

Applicants wish to thank the Examiner for considering the present application. In the Office Action dated October 7, 2005, Claims 1-24 are pending in the application. Applicants respectfully request the Examiner for a reconsideration of the rejections.

Applicants submit herewith a two- month extension of time up to and including March 7, 2006.

Claims 1, 3-6, 8-12, 14-19, and 21-24 stand rejected under 35 U.S.C. §102(e) as being anticipated by *Heile* (6,289,315). Applicants respectfully traverse.

Claim 1 is directed to a method for managing electrical schematic data comprising creating a logical schematic for a part, creating a layout schematic for the part, and creating a physical schematic for the part. Claim 1 further recites associating the logical schematic, the layout schematic, and the physical schematic together to form a part master file. The part master file is stored on a computer network. Claim 1 further recites providing access to the part master file to a plurality of user locations and controlling modification of the part master file so that only one of the plurality of user locations is allowed to modify the part master file at a time.

Applicants respectfully submit that forming a part master file from a logical schematic, a layout schematic and a physical schematic is not set forth in the *Heile* reference. The Examiner point to Col. 6, lines 54-55, and Col. 7, lines 14-22, for creating a logical schematic for a part. However, it appears from these passages that a high level template is set forth and not a logical schematic for the part. Therefore, it appears that this element is not set forth in these passages.

The Examiner points to Col. 7, lines 49-52, for creating a layout schematic. This paragraph is important in understanding the *Heile* application. This paragraph provides examples of different types of designs. For example, a traditional integrated circuit design is set forth that includes a layout versus schematic check. For printed circuit boards automatic routing is performed. The Examiner then points to Col. 5, lines 41-47, for linking all three of the logical layout and physical schematics together in a parts master file. Col. 5, lines 41-47, mentions different types of project files that are associated together. There is no mention of combining the logical schematic, layout schematic and physical schematic together to form any of the project files. In fact, the teachings of Col. 7, lines 49-53, appears to teach away from linking all three of the types together. That is, depending on the specific type of application, more than one of the types may be used but not all three. Therefore, Applicants respectfully request the Examiner to reconsider the rejection of Claim 1.

Claim 11 is directed to a system for managing electrical schematic data. Like Claim 1, Claim 11 also includes forming a part master file that associates the logical schematic, layout

schematic and physical schematic together. Claim 19 is directed to a method claim that also sets forth creating a physical schematic in a single file that includes the logical schematic, layout schematic and physical schematic. Applicants therefore respectfully request the Examiner to reconsider the rejection of Claims 11 and 19 for the same reasons set forth above with respect to Claim 1.

Claims 3-6, 8-10, 12, 14-18, and 21-24 depend from there respective independent claims and are also believed to be allowable for the same reasons set forth above.

Claim 7 stands rejected under 35 U.S.C. §103(a) as being unpatentable over *Heile* in view of *Van Huben* (6,094,654). Applicants respectfully traverse.

Applicants admit that a pointer is set forth in the *Van Huben* reference. However, the *Van Huben* reference does not teach or suggest the further step of storing a pointer in the part master file wherein the pointer indicates a storage location of the logical schematic, physical schematic and layout schematic. In fact, there is no teaching or suggestion in the *Van Huben* reference for associating the three types of schematics, logical, layout and physical together in one file. Applicants therefore respectfully request the Examiner to reconsider the rejection of Claim 7 as well.

Claims 3, 13 and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Heile* in view of *Tou* (Knowledge-Based Approach for the Verification of CAD Database Generated by an Automatic Schematic Capture System). Applicants respectfully traverse.

As the Examiner points out, the *Heile* reference fails to teach using the logical schematic, physical schematic and layout schematic to form a schematic image file. The Examiner points to the *Tou* reference for disclosing the method that uses schematics of a design to form schematic image files. Although a CAD system is set forth, no teaching or suggestion is provided for creating a part master file from a logical schematic, layout schematic and physical schematic. Applicants therefore respectfully request the Examiner to reconsider the rejection of Claims 3 and 20 as well.


Claim 13 recites that the part master file comprises a schematic image file based upon the three different types of schematics. As mentioned above, there is no teaching or suggestion for linking the three types of files or for the presence of the three types of files in the *Tou* reference. Applicants therefore respectfully request the Examiner to reconsider the rejection of Claim 13 as well.

In light of the above amendments and remarks, Applicants submit that all objections are now overcome. Applicants respectfully submit that the application is now in condition for

allowance and expeditious notice thereof is earnestly solicited. Should the Examiner have any questions or comments the Examiner is respectfully requested to call the undersigned attorney.

Please charge any fees required in the filing of this amendment to Deposit Account 06-1510.

Respectfully submitted,



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